A Novel Scheme to Eliminate Common Mode Voltage in Multilevel Inverters

Nasim Rashidi-rad, Abdolreza Rahmati, Adib Abrishamifar

Abstract—Nowadays, multilevel voltage source inverters offer several advantages compared to their conventional two-level inverters. In these inverters, by synthesizing several levels of dc voltages, the staircase output waveform is produced. The structure of this waveform will have lower total harmonic distortion which leads to an approach to a desired sinusoidal waveform. Achieving higher output voltage and lower stress on power switches are other advantages of theses inverters. But in multilevel inverters the problem of common mode voltage which had been found in conventional two level inverters can still be considered as a major issue which leads to motor bearing failures. Therefore to eliminate these voltages proposing some methods seems to be necessary. This paper proposes a generalized method to generate pulse width modulation signals in multilevel inverters that have an odd number of levels. The main idea of this method to generate these signals for an n-level inverter is based on a freely selectable modulation method of an (N+1)/2 level imaginary inverter. This method which leads to eliminate common mode voltages of the n-level inverter can be extended to higher levels.

Index Terms— Common mode voltage, Phase voltage, Line voltage, N level inverter.

1 INTRODUCTION

Multilevel inverters are receiving increased attention recently, especially for use in high power applications. This increased attention is probably due to the fact that the output waveforms are much improved over those of the two level inverters.

The staircase waveform of multilevel inverters which is composed of several levels of dc voltages, will lead to higher output voltage and lower stress on power switches. Furthermore by increasing the levels of output voltage, the waveform contains lower harmonic contents that will lead to reduce the requirements of output filter.

Therefore multilevel inverters have been selected as a preferred power inverter topology for high voltage and high power applications [1-4].

All multilevel PWM inverters such as conventional two level inverters generate common-mode voltage within the motor windings. This voltage may result in motor and drive application problems [5].

This paper presents a method in multilevel inverters, which is based on space vector diagram in an imaginary inverter. This scheme completely eliminates common-mode voltages and will be applicable for any general circuit configuration.

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The following sections of the paper present the algorithm of this method and simulation results in a five level inverter.

2 PRINCIPLES OF THE PROPOSED METHOD

In an N-level inverter, each phase voltage can produce an N-level staircase waveform. Therefore line voltages of this inverter which is the subtraction of two phase voltages will have 2N-1 levels.

$$\begin{aligned} V_{ab} &= V_a - V_b \\ V_{bc} &= V_b - V_c \\ V_{ca} &= V_c - V_a \end{aligned} \quad (1)$$

The average of line voltages with 120 degree phase difference will be zero at each moment.

$$V_{ab} + V_{bc} + V_{ca} = (V_a - V_b) + (V_b - V_c) + (V_c - V_a) = 0 \quad (2)$$

Therefore if line voltages of one imaginary inverter will be used as phase voltages of another inverter, the momentary average of the phase voltage of the second inverter will be always zero. To achieve this, the following equations are necessary to be valid in the system:

$$if \ V_{Line\,(N_I\ Level)} = V_{Phase\,(N\ Level)} \Rightarrow \begin{cases} 2N_I - 1 = N \\ \sqrt{3}(N_I - 1)V_{C\,(N_I\ Level)} = (N-1)V_{C\,(N\ Level)} \end{cases} \quad (3)$$

$$\Rightarrow V_{C\,(N_I\ Level)} = \frac{(N-1)V_{C\,(N\ Level)}}{\sqrt{3}(N_I - 1)}$$

Therefore it can be concluded that if line voltages of an (N+1)/2 level inverter will be used as phase voltages of an N level inverter, then the common mode voltage of the N level inverter will become zero.

In other words, each voltage vector in the space vector diagram of the (N+1)/2 level inverter will be corresponded to the voltage vectors with zero common mode voltage in an N level inverter. Therefore the number of all voltage vectors in an (N+1)/2 level inverter is equal to the number of voltage vectors with zero common mode voltage in an N level inverter.

It should be noted that since (N+1)/2 is an positive integer number, N cannot become an even number; this means that for an even N, an N level inverter cannot have zero common mode voltage.

In the following paragraphs, the relations between number of vectors and switching states for an N and (N+1)/2 level inverters has been presented.

Based on table 1, the number of switching states in a three phase N level inverter will be N^3. Among these states, the number of voltage vectors will be calculated based on following relations.

$$N_{V(N=1)}=1,\ N_{V(N)}=N_{V(N-1)}+6(N-1)\ \Rightarrow \\ N_{V(N=2)}=7,\ N_{V(N=3)}=19,\ldots \quad (4)$$

Therefore the number of voltage vectors with zero common mode voltage in an N level inverter can be calculated as:

$$N_{Vectors\ With\ Vcom=0(N)}=N_{V((N+1)/2)} \quad (5)$$

3 RESULTS

This scheme has been explained for a 5level modular inverter, which has been utilized to drive a 400 volt motor. Therefore the space vector diagram which has been used, belongs to the 3level inverter and $V_{C_{TOTAL}}=600v$.

$$if\ \ V_{Line(3level)}=V_{Phase(5level)}:$$
$$2V_{C(3level)}=\frac{4V_{C(5level)}}{\sqrt{3}}\ \Rightarrow\ V_{C(3level)}=\frac{2V_{C(5level)}}{\sqrt{3}} \quad (6)$$
$$V_{C_{TOTAL}}=(N-1)V_{C(N\ Level)},\quad N=5\ \Rightarrow$$
$$V_{C(5level)}=150\,v\ \Rightarrow\ V_{C(3level)}=173.2v$$

TABLE I. RELATIONS BETWEEN NUMBER OF VECTORS AND SWITCHING STATES

N	NUMBER OF SWITCHING STATES IN AN N LEVEL INVERTER	NUMBER OF VOLTAGE VECTORS IN AN N LEVEL INVERTER	NUMBER OF VOLTAGE VECTORS WITH VCOM=0 IN AN N LEVEL INVERTER	NUMBER OF VOLTAGE VECTORS IN AN (N+1)/2 LEVEL INVERTER	NUMBER OF SWITCHING STATES IN AN (N+1)/2 LEVEL INVERTER
1	1	1	1	1	1
3	27	19	7	7	8
5	125	61	19	19	27
7	343	91	37	37	64

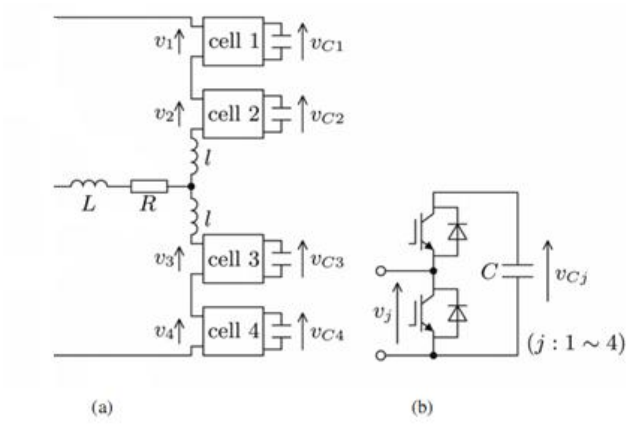


Figure 1. Circuit configuration of (a) one phase leg of a five level modular inverter, (b) a half-bridge cell

According to the proposed scheme, phase voltages of the 5level inverter will be composed by line to line voltages of the 3level inverter. So in these equations V_a, V_b and V_c are phase voltages and:

$$V_{a(5level)}=V_{a(3level)}-V_{b(3level)}$$
$$V_{b(5level)}=V_{b(3level)}-V_{c(3level)} \quad (7)$$
$$V_{c(5level)}=V_{c(3level)}-V_{a(3level)}$$

The definition of the common mode voltage is:

$$V_{com(5level)}=\frac{V_{a(5level)}+V_{b(5level)}+V_{c(5level)}}{3}\ \Rightarrow \quad (8)$$

Therefore:

$$V_{com(5level)}=0 \quad (9)$$

Considering the elimination of common mode voltage in the 5level inverter, it can be concluded that it won't be dependent to the modulation method which is utilizing in the imaginary 3level inverter.

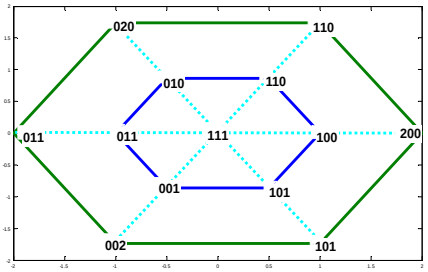
Another conclusion is that redundant switching states as shown in figure 2, will have similar results. For instance if the selected modulation method in 3level inverter will be based on delivering nearest vector to the reference vector, election each of switching states of (2,1,1) or (1,0,0) will lead to zero common mode voltage and equal output voltages in the 5-level inverter. Furthermore among three switching states for zero vector, the vector of (1, 1, 1) has been selected.

In this stage, selecting a suitable modulation method in the imaginary 3level inverter, that has a rather low harmonic distortion and a good linearity relationship is highly important. But it should be noted that reducing or eliminating of common mode voltage in the selection of the modulation method won't be considered.

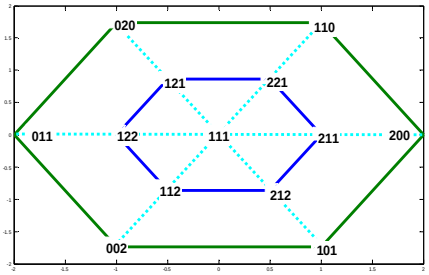
Therefore one of the major advantages of the proposed method is its independency in selection of modulation method of the (N+1)/2 level inverter.

Since elimination of common mode voltage in SPWM methods usually is more difficult than SVM methods, the proposed scheme can be utilized to eliminate the common mode voltage in SPWM methods. Figure 4 has shown phase and line and also common mode voltage in the 5level inverter utilizing an SPWM method.

It should be noted that the selective carrier based modulation is PD (Phase Disposition) method, which has the same phases of two adjacent carriers [6].



(a)



(b)

Figure 2. Considering of redundant switching states in space vector diagrams of the 3level inverter

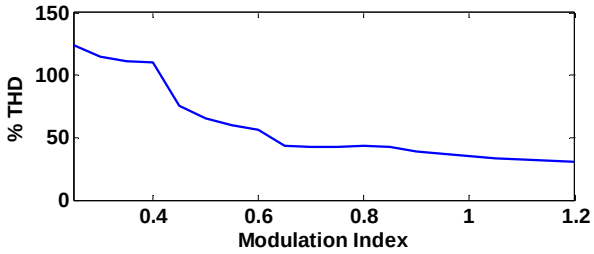
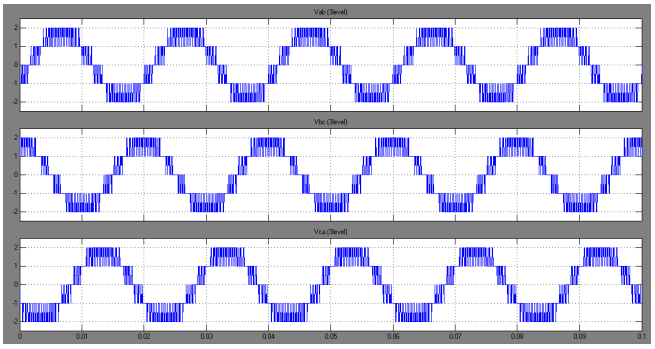
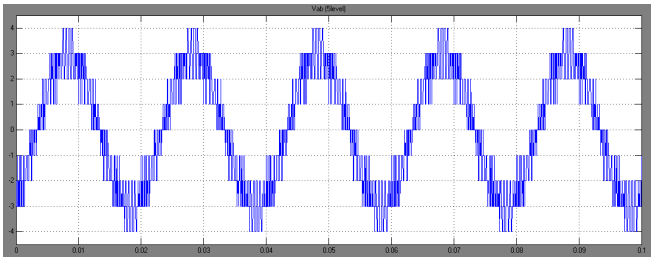


Figure 3. Total harmonic distortion in the 5level inverter, for both diagrams of figure 2



(a)



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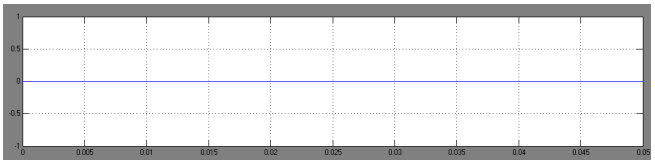

(C)

Figure 4. (a) phase voltages, (b) line voltage, and (c) common mode voltage in the 5level inverter by an SPWM method (PD)

4 Conclusion

This paper has proposed a novel scheme to generate pulse width modulation signals for multilevel inverters. This scheme which can be used in inverters with an odd number of levels will reduce the common mode voltage to zero.

The main idea of the scheme is based on zero momentary average of line voltages in each inverter. Therefore by

utilizing the line voltages of an imaginary inverter as phase voltages of the real inverter, the common mode voltage of the real inverter will be zero.

Furthermore it can be concluded that the number of all voltage vectors in the imaginary inverter will be equal to the number of voltage vectors with zero common mode voltage in the real inverter.

Independency of this scheme in selection of SPWM or SVM methods for the imaginary inverter is one of its major advantages.

The proposed method has been shown for an inverter with 5level voltage. It should be noted that this method can be easily extended to higher levels.

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